Student Achievements & Alumni contributions:

1. MTech VLSI final year students received internship in Vertiv (2 students), Philips (1 student), Cyient (2 students; analog), TGC crest (One student; battery design)
2. Students from JU participated in Synopsys SNUG in Bangalore on 18th July 2024. One faculty, two UG ETCE and one MTech VLSI students have been invited to present two works under academic track.
3. Three M Tech VLSI students have participated in DVCON India 2024 design contest. They shortlisted upto the final among top 10 teams.
4. Two Students (One MTech VLSI and One UG ETCE) have shortlisted for zonal, regional round of Anveshan 2023. First round in JU, next round in Northeastern Hill University Shillong and shortlisted for final round in IIT Bombay. Their work is based on 3D MRI implementation and algorithm demonstration in FPGA and Rasp PI board.
5. One student from UG EE has been selected as one of the top 3 poster presentations for Global SARA day 2024 on 16th September 2024
6. One student from UG EE has been selected as a summer research intern at Dept. of CSE, IIT KGP (Prof. Debdeep Mukherjee) based on her technical knowledge gathered by working in Digital VLSI design laboratory.
7. Two students from UG EE have successfully completed the level 1 training of India Semiconductor workforce development program (ISWDP) organized by IISC Bangalore in collaboration with Synopsys from 1st March to 15th March 2024.
8. Two students (UG EE and UG ETCE) have reached the final of the student poster contest 2024 organized by IEEE Solid State Circuit society Kolkata chapter on 27th October 2024
9. PG curriculum of Jadavapur University Engineering and Technology has been revised and inline to that PG curriculum of JU ETCE has also modified inline to MoU with Synopsys and subsequent suggestions received from stakeholders.
10. Purchase of one workstation [HP z2 G9], 24 Port GigaB Switch (2), PYNQ Z2 board (1), Jetson Nano development kit (2), NVidia GeForce RTX3060 12 GB GPU (1), NVidia RTX 4060 Ti 16GB Graphics card (1), 16 i5 PC and 2 i7 PC has been completed. Purchase of Synopsys full tool bundle (5 Asia Pac FE, 5 Asia Pac BE and 5 Asia Pac Full custom 3 years Floating license has also completed.
11. Two MTech VLSI students (as a team) have shortlisted among the problem statement received throughout India by Western digital design competition at Bengaluru for the Track: Digital circuits and systems design. Topic of Design: design

of flash memory cells as synaptic elements for neuromorphic computing. Only 10 teams were selected by Western digital from all over India, and Jadavpur University was one of them

12. Representatives from Cadence (Hyderabad center) visited JU campus for future collaborative project-based mentorship work. Discussion held on ETCE syllabus specifically on the domain of Analog.
13. Collaboration initiated with Indian Association for the Cultivation of Science on Quantum cold interaction. Primary requirements from JU side are to provide design support on 30 channel pulse generator and delay circuit which will be used for cold chemistry molecular study. Three UG students are working along with the IACS research scholars. Moreover, the programming process of currently purchased 21 channel pulse generators are also taken care of by them.
14. Collaboration with CGCRI on FPGA based neuromorphic works are taken care where three UG students (ETCE and EE) are sitting with scientists of CGCRI for FPGA based work. Initially image processing techniques in hardware are taken care of.
15. Two MTech VLSI students and One UG EE students are mentored by alumni (INTEL) for working on multiplier design from design level towards layout design.
16. Student members of Digital VLSI Club showcased their works during student exhibition held in JU from 11th September to 13th September 2024 as a part of NAAC visit. NAAC pear team experts interacted with them. Incidentally NAAC team visited IC CoE. Observations pointed out the quality of old instruments housed in microelectronics labs.
17. Inc42's latest report estimates that India's semiconductor market will reach $150 Bn by 2030, up from $33 Bn in 2023. As India sets its sight on becoming a chip-making superpower. Jadavpur University has been listed as one of the key enablers of this progress.
18. The summer internship program offered by IC CoE has been completed from May to August. Two batches on the Microelectronics course (total 145 students) One batch on Embedded IoT course (56 students).
19. Recruitment companies related to VLSI, semiconductor: Synopsys (3), Ixana(2), Micron (5), Ti (10), Juniper (coming on 6th November)
20. Discussions with Maven Silicon have been initiated for RISC V training. The initiative has been started with the support of Alumni (Arghajit Basu)
21. JU EE Alumni has initiated to set up a FPGA lab under IC CoE. BoM for the FPGA lab is under preparation.
22. Two Digilent Nexys A7-100T boards are donated by Jayanto Bose (BETCE'95) and implementation overseen by Kishalay Halder (BETCE'95) for interfacing Open Lane for the work on RISC V ISA. In the words of Mr. Kishalay Halder, one of the Board of Observer members for IC-COE:

a. “Though RISC-V is nothing new and loads of universities have already implemented the ISA, JU has kept herself aloof from this worldwide phenomenon unfortunately. This kind of open CPU hardware opportunity comes once in a lifetime but apparently JU ETCE department was not participating in this wave. Furthermore, Open Lane, an open-source EDA toolchain and OpenFlow, an open-source backend flow are also crystallizing with Participation of many Universities and patronage of Google. JU had not participated in this wave either.

   With Sayan's help and eagerness, we decided to touch both with a single project. Create a RISC-V processor ground up and implement with OpenLane/OpenFlow PDK. To keep the learning curve honest, we decided not to take help from any existing, freely available RISC-V cores, but learn from square one with mistakes welcome.

   We started with RISC-V ISA study just a few months back and are about to start the RTL simulation stage using OpenLane toolchain. However, I was feeling the void of a suitable Emulation platform that would give the project the opportunity to create a small SoC testing harness once the processing pipeline is implemented.

   Since Sayan and his scholars have experience with Vivado environment, I decided to fund two Digilent Nexys A7-100T boards. These boards are easily available in US directly from Digilent. When I asked in JUETCE-95 group if anybody was planning to travel to India soon, Jayanta Bose (CA) stepped up and offered to fund both boards himself. He procured and shipped two boards to Arnab Majumdar in NJ, who was planning to visit Kolkata in Aug'24. However, due to personal circumstances his plan got cancelled. This time Sumanesh Samanta offered to carry these boards in October'24. Arnab shipped the boards to Sumanesh (in CO), who carried it to Kolkata. Sumanesh wanted to visit the lab and handover the boards personally to Sayan but JU got closed due to Cyclone Dana exactly during his visit. He then couriered the boards to Sayan.

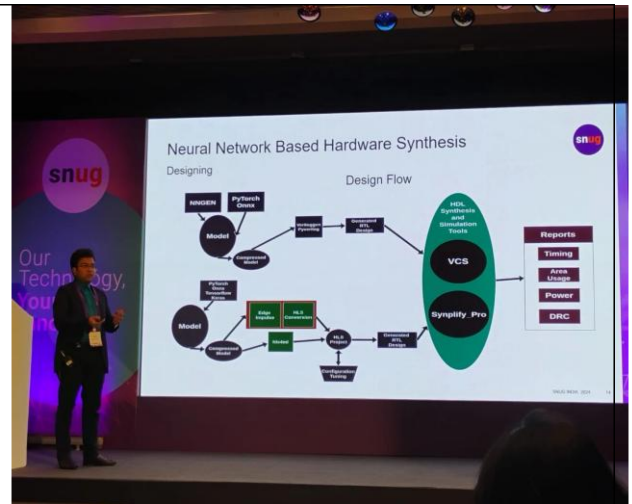
   This is a great example of how any Alumni can contribute directly to selected projects in his/her own department, using our worldwide network and coordination.”

23. Participation of UG, PG students and PhD scholar in Bigyan Mela organized by Paschim Bangla Bigyan Mancha besides Scottish Church College premises showcasing the following models:

    i) Arabic Sign Language Recognition and Voice Translation Device Using Embedded Machine Learning

    ii) Weed Detection and Removal Rover for Precision Agriculture

24. Development of IoT based Fish Water Environment Monitoring System for Fish Cultivation developed by a team of PG and PhD students has received JU innovation seed grant.
25. Organization and conduction of 1 month summer internship course for UG students from various technical institutions on “Embedded Systems and IoT” during July 2-August 2, 2024.
26. Lecture workshop
    a. Evaluation of CMOS AMS/RF over three decades by Mrinal das, Synopsys, 31st July 2024
    b. Technical Lecture on “Emerging interconnects” and “ Device modeling” by Sourajeet Roy and Avirup Dasgupta, Dept. of ECE, IIT Roorkee on 29th February 2024.
    c. DESIGN AND PROTOTYPING FOR FPGA/SoCs WITH MATLAB & SIMULINK
    By Dr. Anand Mukhopadhyay, Senior Engineer - Education Team, MathWorks India Pvt. Ltd., Bangalore, 22nd August 2024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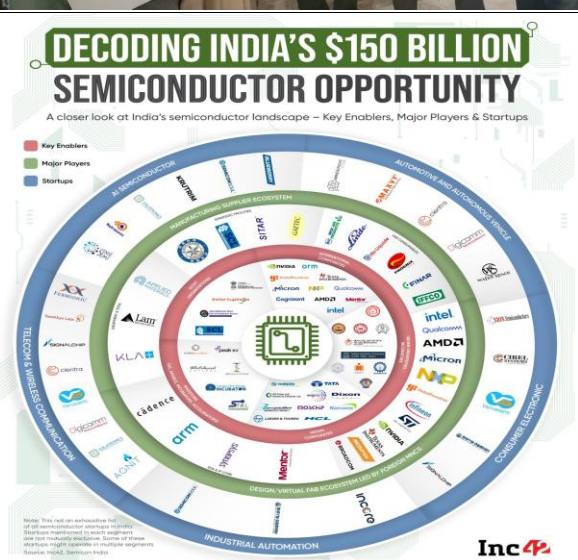
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A closer look at India's semiconductor landscape – Key Enablers, Major Players & Startups
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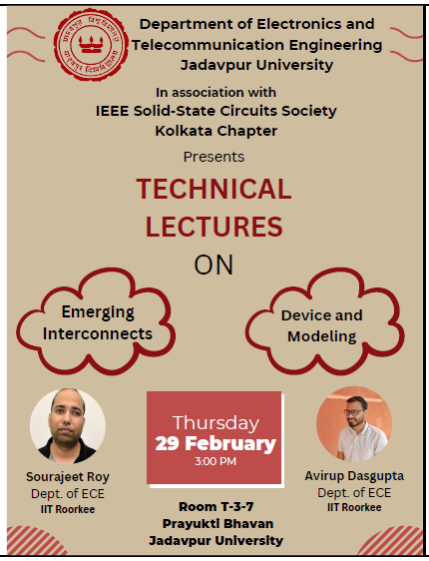
Department of Electronics and Telecommunication Engineering
Jadavpur University
In association with
IEEE Solid-State Circuits Society
Kolkata Chapter
Presents
TECHNICAL LECTURES
ON
Emerging Interconnects
Device and Modeling
Sourajeet Roy
Dept. of ECE
IIT Roorkee
Thursday
29 February
3:00 PM
Avirup Dasgupta
Dept. of ECE
IIT Roorkee
Room T-3-7
Prayukti Bhavan
Jadavpur University