WORSKSHOP ON SYSTEM VERILOG

A value added course

Organized by

Digital VLSI Club

In Digital VLSI Laboratory

Using

SYNOPSYS®

JADAVPUR UNIVERSITY

188 RAJA SUBODH CHANDRA MALLICK ROAD

KOLKATA: - 700032

WORKSHOP BASED ON SYSTEM VERILOG AND OOPS : -

✓ *Attendance Sheet: -*

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✓ *Images of the workshop : -*

Brief about the workshop : -

Delivered the lecture on System Verilog, OOPS and Data Structure and Algorithms. Also those who have not got the knowledge to use the tool they got the opportunity to learn.

Course module

The training module on SystemVerilog and Object-Oriented Programming (OOPs) is a pivotal addition to the standard curriculum, offering students a comprehensive understanding of cutting-edge technologies essential for modern engineering practices. SystemVerilog, a hardware description and verification language, enables students to delve into the intricacies of digital design and verification, equipping them with industry-relevant skills crucial in fields like VLSI design and FPGA development. Moreover, incorporating Object-Oriented Programming principles within SystemVerilog empowers students to leverage robust design methodologies, fostering code reusability, maintainability, and scalability. By integrating these advanced concepts into the curriculum, students not only gain proficiency in foundational engineering principles but also acquire practical expertise sought after by leading technology companies, thus enhancing their employability and paving the way for a successful career in the ever-evolving field of engineering.

Module 1: Introduction to SystemVerilog and OOPs

- Introduction to SystemVerilog and its role in digital design and verification.
- Basics of Object-Oriented Programming (OOPs) principles.
- Overview of Synopsys tools: VCS for simulation, Design Compiler for synthesis, and Formality for formal verification.

Module 2: SystemVerilog for Digital Design

- SystemVerilog data types, operators, and procedural blocks.
- RTL design using SystemVerilog constructs.
- Synthesis-friendly coding guidelines and optimization techniques.

Module 3: SystemVerilog for Verification

- Functional verification methodologies: Directed testing, Constrained Random Testing, and Coverage-driven verification.

Module 4: Advanced Topics in SystemVerilog

- SystemVerilog Assertions (SVA) for formal verification.
- Transaction-Level Modeling (TLM) for high-level verification.
- Introduction to DPI (Direct Programming Interface) for interfacing SystemVerilog with C/C++.

Module 5: Integration with Synopsys Tools

- Integrating SystemVerilog designs with Design Compiler for synthesis.
- Timing analysis and optimization using Design Compiler.
- Formal verification using Formality.

Trainers : -

- Rikta Pal (M.Tech in VLSI Design and Microelectronics Technology)
- Adway Paul (UG ETCE)
- Himanshu Shaw (UG ETCE)

Date :- 12th January 2024

Time :- 11:00 am to 4:30 pm

Brochure image:-