VLSI GURU WORKSHOP

A value added course

In Digital VLSI Laboratory

Using

SYNOPSYS®

JADAVPUR UNIVERSITY

188 RAJA SUBODH CHANDRA MALLICK ROAD

KOLKATA: - 700032

❖VLSI Guru Workshop : -

Name	Course
Rikta Pal	M.Tech in VLSI Design and Microelectronics Technology
Adway Paul	B.E in ETCE
Himanshu Shaw	B.E in ETCE
Subha Bhattacharya	B.E in EE
Ankit	B.E in IEE
Gulshan Poddar	B.E in IEE

Brief about the workshop : -

The VLSI Guru Workshop stands as a premier opportunity for participants to immerse themselves in an intensive exploration of VLSI design, emphasizing the utilization of Synopsys tools like Synplify Pro, VCS, and Verdi. Synplify Pro serves as a cornerstone for synthesis, enabling participants to delve deep into the process of transforming RTL descriptions into optimized gate-level representations suitable for implementation on silicon. Through hands-on exercises and guided tutorials, participants gain proficiency in harnessing Synplify Pro's advanced features for achieving design closure and maximizing performance. Complementing synthesis, VCS facilitates rigorous functional verification through robust simulation capabilities. Workshop attendees learn to create comprehensive testbenches, simulate complex designs, and analyze results using VCS, ensuring the reliability and correctness of their VLSI implementations. Additionally, Verdi emerges as an indispensable tool for debugging and visualization, empowering participants to navigate through intricate design hierarchies, trace signal paths, and identify and rectify potential issues efficiently. Beyond tool proficiency, the workshop

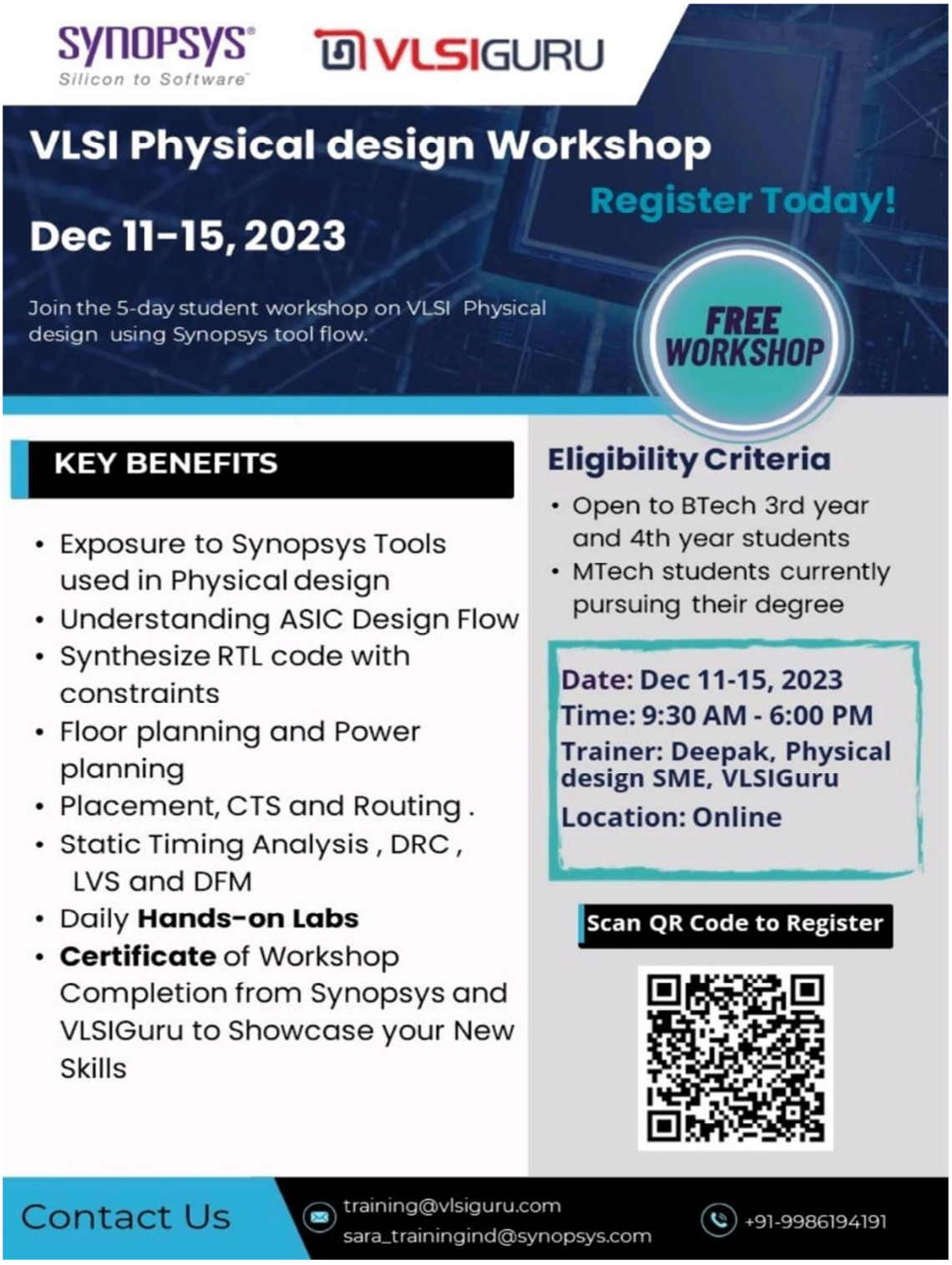
delves into the realm of sequential circuits, with a particular focus on Asynchronous FIFOs. Participants acquire a thorough understanding of asynchronous circuit design principles, exploring techniques for mitigating metastability and ensuring reliable data transfer in high-speed asynchronous communication systems. By combining theoretical insights with practical hands-on experience, the VLSI Guru Workshop equips participants with the skills and expertise necessary to excel in the dynamic field of VLSI design and verification.

The exploration of Asynchronous FIFO design utilizing Synopsys tools represents a significant value addition to the standard digital electronics syllabus. Asynchronous FIFOs play a pivotal role in modern digital systems, facilitating efficient and reliable data communication between asynchronous domains. Through hands-on exercises and guided tutorials, students not only grasp the fundamental principles of asynchronous circuit design but also develop proficiency in utilizing industry-standard tools for synthesis, simulation, and debug. This practical experience enhances students' readiness for tackling real-world engineering challenges in fields like VLSI design, FPGA development, and digital system design. Additionally, the incorporation of Asynchronous FIFO design using Synopsys tools broadens students' skill set, providing them with a competitive edge in the job market and preparing them for success in the ever-evolving realm of digital electronics and embedded systems.

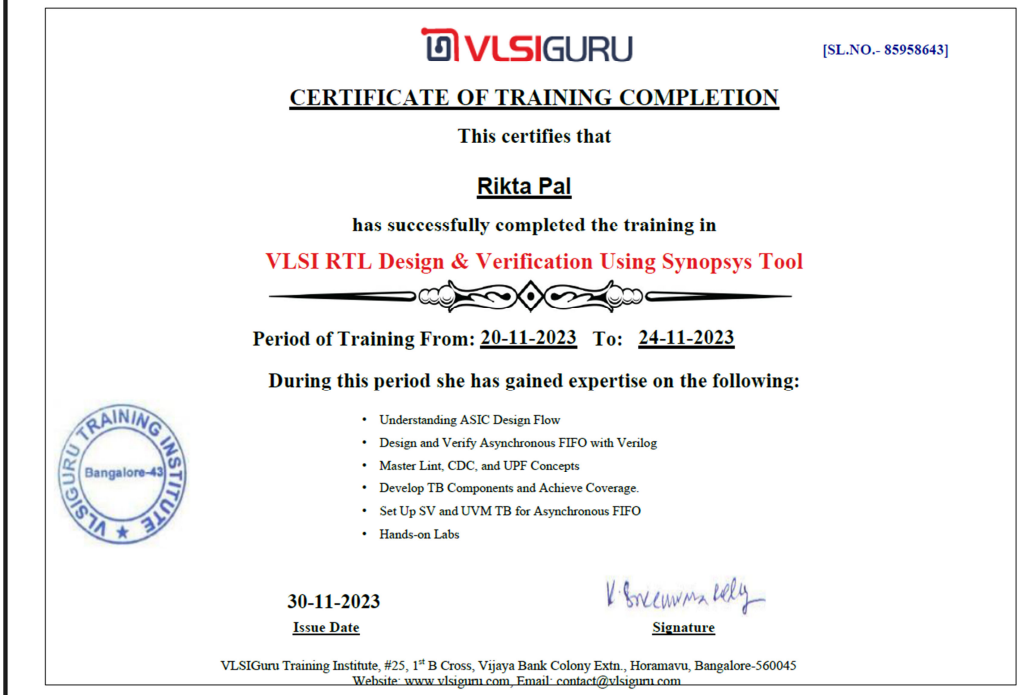
Date :- 11th December to 15th December 2023

Time :- 9:30 am to 6:00 pm

Banner/ brochure image :-



✓ *Images of the certificates : -*



VLSIGURU [SL.NO.- 85958643]

CERTIFICATE OF TRAINING COMPLETION

This certifies that

Rikta Pal

has successfully completed the training in

VLSI RTL Design & Verification Using Synopsys Tool

Period of Training From: 20-11-2023 To: 24-11-2023

During this period she has gained expertise on the following:

- Understanding ASIC Design Flow
- Design and Verify Asynchronous FIFO with Verilog
- Master Lint, CDC, and UPF Concepts
- Develop TB Components and Achieve Coverage.
- Set Up SV and UVM TB for Asynchronous FIFO
- Hands-on Labs

VLSIGURU TRAINING INSTITUTE Bangalore-43

30-11-2023
Issue Date

Signature

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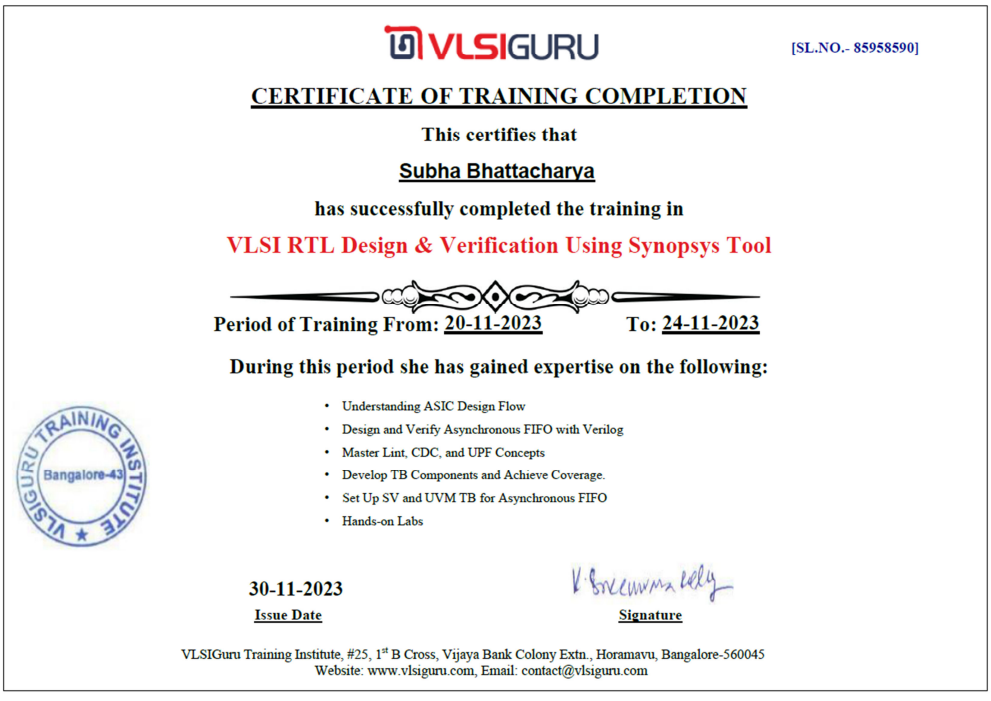
Website: www.vlsiguru.com, Email: contact@vlsiguru.com



VLSIGURU [SL.NO.- 85958590]

CERTIFICATE OF TRAINING COMPLETION

This certifies that

Subha Bhattacharya

has successfully completed the training in

VLSI RTL Design & Verification Using Synopsys Tool

Period of Training From: 20-11-2023 To: 24-11-2023

During this period she has gained expertise on the following:

- Understanding ASIC Design Flow
- Design and Verify Asynchronous FIFO with Verilog
- Master Lint, CDC, and UPF Concepts
- Develop TB Components and Achieve Coverage.
- Set Up SV and UVM TB for Asynchronous FIFO
- Hands-on Labs

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[SL.NO.- 85958587]

CERTIFICATE OF TRAINING COMPLETION

This certifies that

Ankit

has successfully completed the training in

VLSI RTL Design & Verification Using Synopsys Tool

Period of Training From: 20-11-2023 To: 24-11-2023

During this period he has gained expertise on the following:

- Understanding ASIC Design Flow
- Design and Verify Asynchronous FIFO with Verilog
- Master Lint, CDC, and UPF Concepts
- Develop TB Components and Achieve Coverage.
- Set Up SV and UVM TB for Asynchronous FIFO
- Hands-on Labs

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[SL.NO.- 85958619]

CERTIFICATE OF TRAINING COMPLETION

This certifies that

Himanshu Shaw

has successfully completed the training in

VLSI RTL Design & Verification Using Synopsys Tool

Period of Training From: 20-11-2023 To: 24-11-2023

During this period he has gained expertise on the following:

- Understanding ASIC Design Flow
- Design and Verify Asynchronous FIFO with Verilog
- Master Lint, CDC, and UPF Concepts
- Develop TB Components and Achieve Coverage.
- Set Up SV and UVM TB for Asynchronous FIFO
- Hands-on Labs

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VLSIGURU

[SL.NO.- 85958582]

CERTIFICATE OF TRAINING COMPLETION

This certifies that

Adway Paul

has successfully completed the training in

VLSI RTL Design & Verification Using Synopsys Tool

Period of Training From: 20-11-2023 To: 24-11-2023

During this period he has gained expertise on the following:

- Understanding ASIC Design Flow
- Design and Verify Asynchronous FIFO with Verilog
- Master Lint, CDC, and UPF Concepts
- Develop TB Components and Achieve Coverage.
- Set Up SV and UVM TB for Asynchronous FIFO
- Hands-on Labs

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