Handson Training on Synopsys tools

And

Design of a CPU

A value added course

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JADAVPUR UNIVERSITY

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KOLKATA: - 700032

SYNOPSYS WORKSHOP

Attendance Sheet: -

Name	Course
Rikta Pal	M.Tech in VLSI Design and Microelectronics Technology
Sayan Chatterjee	M.Tech in VLSI Design and Microelectronics Technology
Adway Paul	B.E in ETCE
Himanshu Shaw	B.E in ETCE
Soham Paramanik	B.E in ETCE
Sourin Karmakar	M.Tech in VLSI Design and Microelectronics Technology
Akash Bose	M.Tech in VLSI Design and Microelectronics Technology
Saheli Ghosh	M.Tech in VLSI Design and Microelectronics Technology
Ankit	B.E in IEE
Gulshan Poddar	B.E in IEE
Pulak Majumdar	PhD
Suraj	B.E in IEE
Rudrajeet Ghosh	M.Tech in VLSI Design and Microelectronics Technology

Date : 16-18th August 2023.

Brief about the workshop : -

The recent Digital VLSI lab inauguration event marked a significant milestone for our academic journey, but it was the concurrent training on Synopsys tools—Synplify Pro, VCS, and Verdi—that truly elevated the learning experience. Over the course of the workshop, we delved deep into the intricacies of these industry-standard tools, gaining invaluable insights into simulation methodologies, timing analysis concepts like setup time, hold time, slack, and clock skew. Moreover, the workshop served as a platform for honing our skills in Verilog and SystemVerilog, essential languages for modern VLSI design. The highlight of the training was the two-day session conducted by industry experts, where we received firsthand knowledge and practical tips on utilizing these tools effectively.

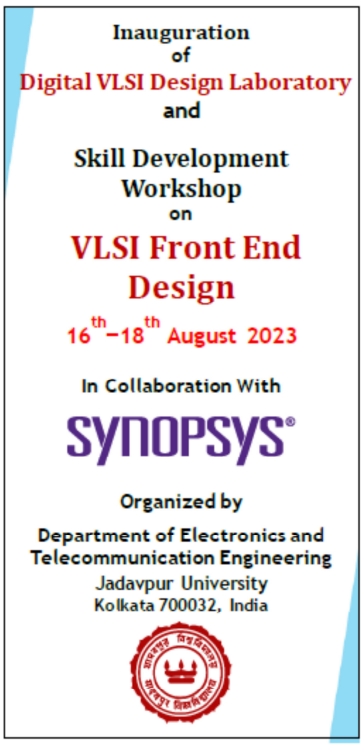
The hands-on approach adopted during the workshop enabled us to solidify our understanding of digital design and verification principles. Through completing assignments and undertaking a mini-project, the Tiny CPU, we not only applied theoretical knowledge but also gained proficiency in implementing real-world solutions. This immersive experience went beyond the confines of our regular curriculum, providing us with a holistic view of the VLSI design process.

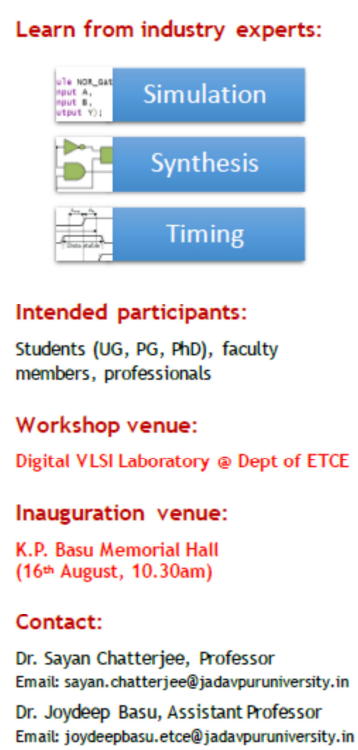
The value added by this training extends far beyond the technical skills acquired. It instilled in us a sense of confidence and preparedness to tackle complex engineering challenges in the professional arena. By bridging the gap between academia and industry, the training equipped us with the tools and knowledge necessary to thrive in the fast-paced field of VLSI design and verification. As we reflect on the inauguration event and the concurrent training, it is evident that this additional learning opportunity has significantly enriched our educational journey, setting a precedent for future endeavors and underscoring the importance of continuous skill development in the ever-evolving landscape of technology.

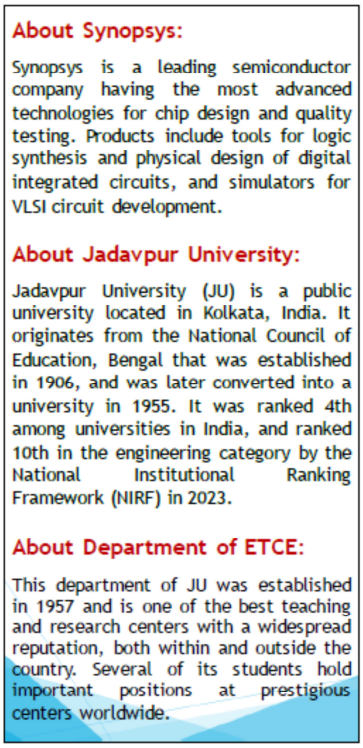
- The Tiny CPU project served as a practical application of the knowledge gained during the training on Synopsys tools and digital design principles.
- Designing the Tiny CPU involved understanding the architecture and functionality of a basic Central Processing Unit (CPU).
- Students gained insights into designing arithmetic and logic units (ALUs), control units, and registers, essential components of a CPU.
- The project necessitated the implementation of sequential logic elements such as flip-flops and state machines.
- Participants learned about instruction set architecture (ISA) and instruction decoding, crucial aspects of CPU design.
- Debugging and verification techniques were applied extensively throughout the project, reinforcing skills acquired during the training.

- Through the Tiny CPU project, students gained practical experience in synthesizing, simulating, and testing a complete digital system.
- Design decisions made during the project, such as optimizing for speed or area, provided insight into trade-offs inherent in digital design.
- The project encouraged collaborative problem-solving and teamwork, fostering communication and project management skills.
- Overall, the Tiny CPU project enhanced participants' understanding of CPU design principles and provided a hands-on opportunity to apply theoretical knowledge in a real-world context, further enriching their educational experience.

✓ *Images of the workshop : -*







About VLSI Design:

Very large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining millions or billions of MOS transistors onto a single chip.

Owing to immense complexity involved in IC design and fabrication, extensive use of design automation and automated logic synthesis tools is required to lay out the transistors. However, certain circuit blocks like analog/mixed-signal are still custom designed to ensure performance.

Knowledge of the various steps of VLSI design flow and related software tools empowers engineers and designers to excel in the dynamic field of electronic design, fostering innovation and driving technological advancements.

Govt. of India's Initiative:

Semiconductor and chip manufacturing has become a national security issue for most countries, propelled by the supply chain shortage of semiconductor chips in recent times. Government of India has identified semiconductors as one of the sectors for growth in its 2030 vision, and has committed to invest $10B in manufacturing incentives. Companies like Micron, Foxconn, Intel, Apple, etc. are planning billions of dollars of investment in India. India has therefore launched a new program called "Chips to Startups" that is intended to produce 85,000 semiconductors-skilled engineers to make India a semiconductor hub.

VLSI Design Activities @ JU ETCE:

Jadavpur University's Electronics and Telecommunication Engineering (ETCE) department has a long legacy as one of the best in Eastern India, with around 40% of its graduates since 1961 working in the field of semiconductors. Faculty members at ETCE are involved in various challenging projects across multiple domains related to VLSI.

About Synopsys VLSI Tools:

Synopsys specializes in cutting-edge electronic design automation (EDA) tools that offer numerous benefits in the ever-evolving landscape of IC design and innovation. Synopsys tools are designed to streamline and optimize various stages of VLSI design and verification, offering a wide range of functionalities, across circuit design, logic synthesis, simulation, and timing analysis.

Synopsys tools cover a broad spectrum of design domains, from digital and analog/mixed-signal design to FPGA prototyping and system-level design. This enables engineers to work on diverse projects and expand their expertise across different areas.

About the Workshop:

This workshop will be conducted by JU ETCE in association with Synopsys India to empower and up-skill students and professionals on digital integrated circuit design and usage of related tools from Synopsys. The following topics relevant for VLSI Front End design will be covered:

1. Verilog RTL and simulation
2. Logic synthesis
3. Timing analysis

Advisory Committee:

Mr. Amit Roy, Director, Synopsys

Dr. Manotosh Biswas, Prof. & HOD, ETCE

Organizing Committee:

Dr. Sayan Chatterjee, Professor, ETCE

Dr. Sheli Sinha Chaudhuri, Professor, ETCE

Dr. Joydeep Basu, Asst. Professor, ETCE