SHORT TERM CERTIFIED SUMMER INTERNSHIP, TRAINING AND MENTORSHIP ON

MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN

Offered by

IC DESIGN & FABRICATION CENTRE
Department of Electronics & Telecommunication Engineering
Jadavpur University, Kolkata – 700032
Website: www.jaduniv.edu.in
E-mail: juiccentre@gmail.com Phone: (033) 2457-2406 / 2414-6217
M: 9830157714, 9903402142

In collaboration with

ELECTRONICS CENTER OF EXCELLENCE
iHub, 2nd Floor, E/43, Infocity Ave, SailashreeVihar
Patia, Bhubaneswar, 751024, India
https://e-coe.co.in

- **4 weeks, Course starts from 1st June, 2023**
- **10.30 AM to 5.00 PM, Monday to Friday**

Admission: Application form will be issued from the IC Centre, Department of Electronics & Telecommunication Engineering, 3rd Floor, Jadavpur University, Kolkata or download from our website [www.jaduniv.edu.in or https://jadavpuruniversity.in]. Filled in application form shall be received at IC Centre during Monday to Friday, 11 AM to 5 PM.

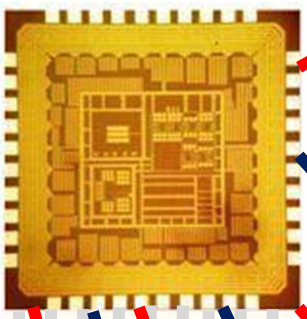
Course Fee:

1) Rupees **7,000/- + 18% GST** in demand draft should be drawn in favour of "**REGISTRAR, JADAVPUR UNIVERSITY**", in any Nationalized branches of payable at Kolkata. Once deposited the course fee cannot be refunded. Hostel accommodation cannot be provided.
2) For ECOE payment please follow the bank details to transfer **2000+18% GST.**

Electronics Center of Excellence
Acct No: 5020004843744
IFSC:HDFC0004013
HDFC Bank, Infocity Branch, Patia, Bhubaneswar - 751024

Enclosure: One copy of PP Size Photograph, Xerox copy of Madhyamik Admit Card / Birth Certificate, HS Mark sheet, Semesters Mark sheet [Attested / Self Attested copies of Mark sheets / Certificates to be enclosed]

Industry orientation for semiconductor companies



Fabrication and Characterization of semiconductor devices

- Mask Fabrication
- Hardware fabrication for all process of Microelectronics: cleaning, oxidation, diffusion, photolithography, etching, and Metallization.
- Characterization of fabricated device.

Verilog Coding for Digital design and FPGA based prototyping

- Basics of Verilog code
- EDA design flow and logic synthesis
- FPGA-based prototyping

CMOS Digital circuits

- Overview of CMOS logic gates
- CMOS based logic circuit
- Layout design
- Fault in digital circuit

VLSI verification Process

- Verification methodology and Verification process
- Reusable TB, Verification environment architecture
- Random coverage driven verification methodology

Analog MOS circuit

- CMOS based analog circuit
- Noise in circuit
- IC Implementation and Layout generation process

VLSI SPICE tool handling

- Introduction to T-SPICE Tools
- Netlist Using T-SPICE and layout design
- Layout Design

Device Physics

- MOS physics
- Short channel effects in deep sub micron technology
- FinFET, GAA FET

Training Bus

Laboratory Facilities